CHIP LEVEL IMPATT COMBINING AT 40 GHz

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ABSTRACT

Results with series and series-parallel connections of CW 40 GHz GaAs IMPATT diodes are discussed. The multichip geometries utilize Raytheon CW double-drift device chips and are essentially scaled versions of successful X-band geometries reported previously [Ref. 1]. Maximum series combining efficiency of 82 percent has been achieved.

Introduction

The authors have reported successful work with series and series-parallel connected IMPATT devices at X-band frequencies.[1] Clearly, it is desirable to extend this technique to millimeter frequencies, if possible. Reported herein is work aimed at scaling the X-band multichip geometries and techniques to 40 GHz. Current results show the approach to be feasible with up to 82 percent combining efficiency; however, high combining efficiency (n_c) has not been repeatably obtained. A possible explanation, related to capacitor loss, for some of the low n_c values is summarized.

Geometries

Figure 1 is a composite sketch showing a typical successful X-band CW device and its nominally equivalent 40 GHz counterpart. The devices are not exactly to scale. Also shown, in Figure 2, is an SEM photomicrograph of a typical two-chip, 40 GHz device.

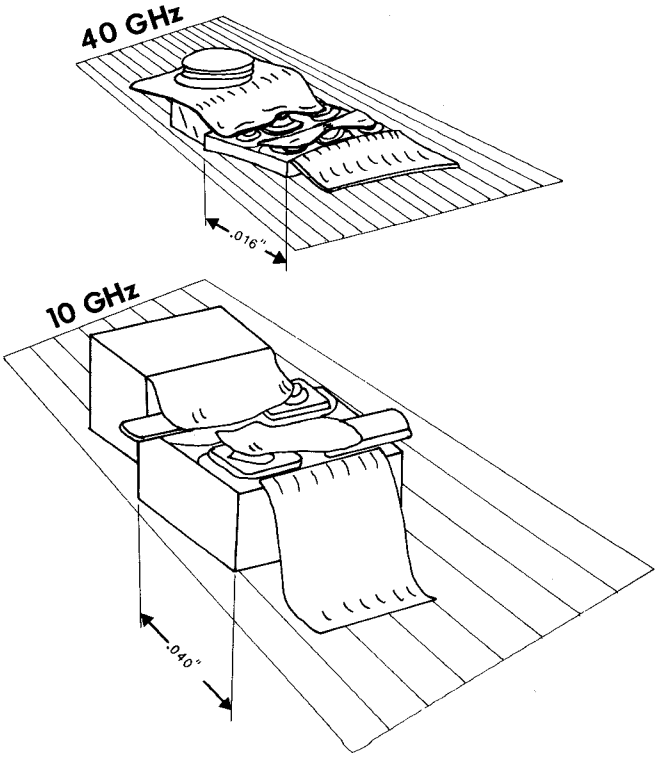

Figure 1. Multichip IMPATT geometries, 40 GHz and 10 GHz.

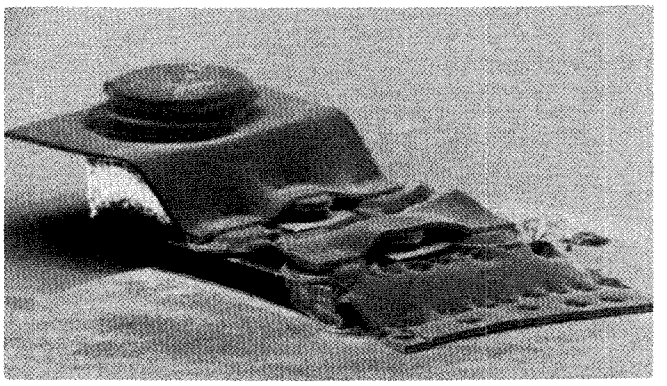

Figure 2. SEM Photomicrograph of 40 GHz Geometry.

In general, all dimensions, including diamond heat sink size, lead lengths, etc. have been held quite close to scale. No identifiable circuit modes related to the size of the geometry have been noted. On the other hand, certain unexplained anomalies noted in performance may nevertheless imply the existence of such modes.

Results

Figure 3 is a summary of significant results to date. A number of packaged devices was tested to establish the nominal efficiency and power to be expected from the available Raytheon device lot. Power and efficiency of .8 watt and 11.2%, respectively, were routinely achieved in a modified Kurokawa-type test fixture supplied by Raytheon. The fixture employs back short, integral E-H tuners and a choke-type bias filter followed by an absorber slug. The lower portion of Figure 3 shows efficiency bounds noted during tests of numerous two-diode series devices. Maximum combining efficiency of 82% and minimum of about 50% have been noted. Clearly, the 82% results are acceptable while values near 50% are not, except in rare instances.

Geometries employing three series chips and two parallel pairs of chips connected in series have also been tested. If circuit losses (as opposed to device losses) lead to the lower efficiencies, the three-chip device would be expected to improve the efficiency by virtue of its higher impedance. A slight improvement was noted at low input power densities but the efficiency degraded rapidly at higher inputs. We have been unable to explain this rapid degradation of performance above inputs of 4 W/chip with the three-chip devices. Experiments with the four-chip series-parallel geometry are also inconclusive. In short, neither the three-chip series device nor the four-chip series parallel device clearly confirms the suggestion that circuit

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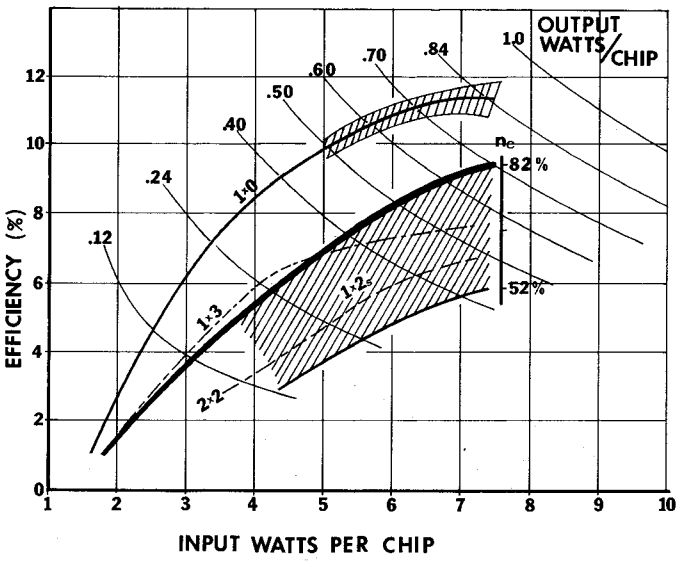

Figure 3. Summary of RF Performance with Multichip Geometries.

losses are a major contribution to low nominal combining efficiency. Possible effects of losses in the multichip device itself are considered next. For discussion purposes, all losses occurring within the multichip device are considered to be "device losses".

Device Losses

To obtain stable operation with series assemblies, it has been necessary to use lumped SiO_2 capacitors in parallel with each diode chip in much the same manner as required for stability (with some devices) in X-band[1]. Deposited thermal oxide and bulk fused quartz capacitors have been used.

We have, in an attempt to explain our results, devised a theoretical treatment which appears to "fit the data". For example, a large signal diode model, based on the analysis of Statz, Pucel, Simpson and Haus[2], was employed. To simulate the double-drift devices used, the impedances of two such devices were added. The physical and material parameters used to characterize the avalanche region and two drift regions were estimated from various Raytheon reports. The results of calculations, using best estimate parameters, are shown in Figure 4. These computed values are a near perfect fit to the measured data of Figure 3 for the range of capacitor Q values shown. The values indicate that circuit Qs as high as 125 significantly affect the efficiency. The reason for this is that the large-signal device model delivers maximum output power at a very low negative resistance, thus resulting in a lower efficiency than one might expect in practice.

At high microwave frequencies, the capacitor Q is almost totally controlled by the conductor loss which is proportional to $f^{-3/2}$. Qs of 50 and 125 at 40 GHz would therefore scale to values of 400 and 1000 at 10 GHz. Using an available 10 GHz large signal analysis with parameters based on measured data, one computes that a Q of 400 at 10 GHz would result in a combining efficiency of 91 percent; a value consistent with X-band performance previously reported. The Q values noted in the foregoing discussion are several times poorer than one would compute based on the bulk

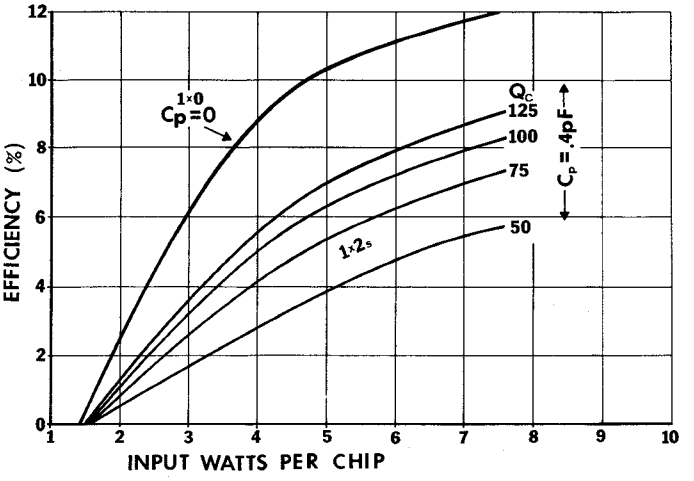

Figure 4. Calculated RF Performance for a Range of Capacitor Qs.

properties of quartz with dense metallizations. Computations based on the work of Young and Sobol[3] give Q values compatible with the range of Q = 50-125 assumed at 40 GHz. DeBrecht[4] has measured Q values of 100 with "highly densified, low-etch-rate" SiO_2 capacitors at 12 GHz. Such a low value would scale to Q = 16.4 at 40 GHz, a value far poorer than those assumed. Therefore, it seems possible that capacitor loss may explain (or more than explain) the observed degradations of efficiency.

Conclusions

A scaling approach has resulted in stable 40 GHz multichip assemblies which do not appear to suffer from problems related to physical geometry such as line length and parasitic effects. Maximum combining efficiency of 82 percent has been obtained but not repeatedly, possibly due to low Q of the stabilization capacitors.

References

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